Aditya B Pattavardhanam

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Electronics and Communication Engineering student focused on VLSI, mixed-signal circuits, and avionics power systems with hands-on experience in RTL design, SPICE-based simulation, and battery management systems.

Education

Bachelor of Technology in Electronics & Communication Engineering — Expected 2027
University of Visvesvaraya College of Engineering (UVCE) — CGPA: 9.07/10(5th sem)
XII - Karnataka State Board — 2023
BASE PU College, Rajajinagar — 91%
X - ICSE — 2021
Daffodils English School — 91%

Skills

Digital Design: RTL using Verilog & SystemVerilog, FPGA (Vivado, Quartus), Digital Logic, Verification Testbenches
Analog/CMOS: CMOS circuit design, SPICE-level circuit analysis, signal conditioning
Embedded & Hardware: PCB Design, Power Electronics
Tools: Vivado, Altium Designer, KiCad, LTspice/Ngspice, MATLAB
Domains: VLSI, Battery Management Systems, Power Management, Avionics
Coding Languages: Verilog, SystemVerilog, SPICE, C/C++, Java, Python

Experience

Project Ūrdhyuth, IISc, Dept. of Aerospace Engineering — Jul 2025 – Present
Non-Linear Multifunctional Composites Analysis and Design Lab
Research Intern – Avionics & Propulsion - **Team Lead(Avionics)**
Guided by Prof. Dineshkumar Harursampath (IISc) and Prof. Ramesh Gupta (NITTR-Bhopal), working on propulsion battery systems and BMS development.

- Developing a Power Management System in MATLAB involving load modeling, protection logic, and subsystem interface definition for an eVTOL platform
- Co-designed Li-Ion NMC battery architecture and implemented Battery Management System functions for monitoring, balancing, and safety protection
- Actively researching Hardware-Based BMS architectures

Incoming Summer Research Fellow — May 2026 – July 2026
Indian Institute of Technology Madras — Department of Electrical Engineering

- Selected for the Summer Fellowship Programme 2026 based on academic credentials
- To work on Integrated Circuit Design

MARVEL UVCE, R&D Lab — Oct 2023 – Present
Coordinator Design & Prototyping | Co-Lead Product Development

- Mentored student electronics designs involving PCB, FPGA, and signal processing
- Co-leading product development cohort focusing on end-to-end hardware solutions
- Co-developed AIR-001 syllabus emphasizing avionics-oriented electronics design
- Authored - ***Before We Scale: Design at the Edge of Intent*** to guide product cohort engineering philosophy

Projects

CMOS Current Mirror Design & Verification(SKY130A, Linux)

- Installed and configured an open-source analog design environment on Linux
- Designed and analyzed a CMOS current mirror, evaluating performance through transient, corner, and Monte Carlo simulations
- Implemented full design flow: schematic, layout, GDS generation, DRC, LVS, and post-layout verification
- Performed parasitic extraction and analyzed deviations between pre- and post-layout behavior
- Automated GDS, DRC, and LVS checks using GitHub Action

HeartGuard – ECG Anomaly Detection Device

- Designed analog front-end using TI ADS1298 (8-channel, 24-bit ECG AFE) with custom signal conditioning for real-time arrhythmia detection

- Developed custom 4-layer PCB in Altium integrating ADS1298, STM32F411 (Cortex-M4), and BLE module for wireless data streaming

Hardware-Aware Spectrum Monitoring with Jammer-like anomaly detection (CMOS Role)

- Built a passive, hardware-aware spectrum sensing platform enabling real-time analysis of channel occupancy and interference patterns using LoRa, FPGA and CMOS analysis
- Designed a transistor-level StrongARM latch comparator in Xschem/Ngspice, achieving 6-7 mV sensitivity and 10 ns decision time under low-amplitude, noise-dominated inputs
- Performed end-to-end validation across noise-only, signal-present, and jammer conditions, demonstrating correct channel occupancy detection and dual-threshold interference classification
- Analyzed system-level behavior including metastability as a functional indicator, detection margins, and transition dynamics between uncertain and deterministic decision regions

Hardware Trojan Detection

- Designed and injected RTL-level hardware trojans in Verilog to model microarchitectural vulnerabilities and study trigger conditions
- Wrote a Verilog testbench instantiating clean and trojan ALU variants simultaneously; applied 70,000 cycles of fixed-seed constrained-random stimulus to detect functional output divergence
- Developed Python-based side-channel detection pipeline using switching activity signatures to identify anomalous RTL behavior

CanSat (Can-Sized Satellite)

- Leading power subsystem design defining power architecture and voltage domains
- Executed power budgeting from component datasheets and duty cycles to size regulators

Technical Writing

- Before We Scale - Design at the Edge of Intent
  - 18-chapter work covering design ethics, abstraction, and hardware-software co-design
  - Authored and used as foundational reading for MARVEL UVCE's Product Development Cohort

Achievements

- 1st Place – MARVEL CTARA Hackathon 2025 - MARVEL UVCE
- 1st Place – Impetus 2025 AvionX Electrical Subsystem – IEEE UVCE
- Winner – SiliconSprint Digital Design Hackathon – IEEE NITK & RVCE
- 1st Place – Kagada 2023 Project Track – IEEE UVCE
- 1st Place – Science Spectrum – Christ University
- Best Performer Award in D-P-001 Level 1 – MARVEL UVCE

Certifications

- VLSI Chip Design and Simulation with Electric VLSI EDA Tool – L&T EduTech / Coursera
- Fundamentals of Digital Design for VLSI Chip Design – L&T EduTech / Coursera
- FPGA Design for Embedded Systems – University of Colorado Boulder / Coursera
- Altium Designer – Altium Education
- ROS 2 Fundamentals – Udemy
- MARVEL UVCE – Level 1 & 2

Volunteering

UVCE Graduates Association Jan 2024 – Present
Podcast Editor and Host – Edited and hosted 13 episodes across seasons 4–6 of UVCE Chronicles
IEEE UVCE – Representative Committee May 2024 – Oct 2024
Coordinator, Power Electronics Society (PELS)

Interests

Performing guitarist and vocalist | Table tennis enthusiast